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3D and Line Scanning Camera System Concept in Real-Time Wood Processing

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***Abstract*— The increasing complexity of modern manufacturing systems requires companies to design and develop a contemporary framework with high degree of accuracy and speed. The demand for precise and fast equipment in wood processing and other industries is topical within modern progress of Machine Learning, more powerful computing systems and approaches. To meet this challenge and to be in pace with Industry 5.0 advancements they rely heavily on real-time systems, which are essential tools for assessing dynamics of manufacturing data. In the paper, the research project focuses on developing an advanced 3D and line-scanning camera system concept for real-time wood defect detection and labelling. High-performance computing (HPC) technologies and FPGA-based (Field-Programmable Gate Array) for real-time processing will be employed to ensure high scanning speed and precision. Additionally, the research will focus on creating the necessary computing algorithms and a set of diagnostic, calibration, and maintenance technologies to optimize the performance and reliability of the scanning system. As the critical step for framework elaboration, the development of a conceptual model for the camera system and evaluation of technological options that would ensure effective recognition of wood defects, as well as creation of a basis for further technological development are performed.**

Keywords*— *Computer Vision, Deep Machine Learning, defect detection, FPGA, HPC, labelling, quality control, wood processing.

I. Introduction

The wood processing sector faces modern challenges coming from the natural variability of wood and the demand for rapid, reliable inspection to reduce waste, improve product quality and increase sustainability [1]. With increasing industrial automation and environmental regulations in Europe, optimizing wood defect detection through real-time imaging and processing is of practical and economic [2], [3], [4].

Despite progress, the problem of accurately and efficiently detecting diverse wood defects in real-time remains unresolved, since the existing approaches vary widely, from traditional image segmentation and texture analysis [5], [6] to deep learning models requiring substantial computational resources [7], [8].

The biggest knowledge gap exists in balancing detection accuracy with processing speed, especially under industrial conditions involving high-speed conveyors and complex defect types [9], [10]. Moreover, the bottleneck exists regarding the optimal hardware platform: FPGA-based systems offer low latency and power efficiency but may lack flexibility, whereas GPU-based and traditional CPU methods provide programmability at the cost of higher power and latency [11], [12], [13]

Research on data processing algorithms through convolutional neural networks (CNNs) and integration with high-performance computing (HPC) in 3D and line scanning camera systems for real-time wood processing has emerged as a critical area of inquiry due to its potential to enhance efficiency and accuracy in defect detection, quality control, and automation within the wood industry [9], [14]. Most of conventional systems were based on common image processing techniques in combination with supervised learning algorithms, however, over the last decade deep learning has achieved remarkable success in the forestry and wood products industry [15], [16]. Deep learning (DL) techniques encompass anomaly detection, feature detection (segmentation), object classification,

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instance segmentation, point localization, and character recognition [17], [18], [19], [20], [21]

As one of the most popular solutions as in recent decades, the industrial sector was focused on efficiency of an industrial vision through automation. The main bottleneck of the process is image processing due to high speed and precision. Graphic processing units (GPUs) and FPGAs have been proposed for real-time detection, where tasks are now performed repeatedly by machines assisting or replacing humans, reducing the occurrence of errors [11], [22], [23]. FPGAs are used to reduce the processing time in vision systems, and consequently, to reduce their cycle time. A real-time image pre-processing system allows filter validation and integration into industrial vision applications. The processing times measured on three platforms show that FPGA execution is faster than both CPU and GPU [11], [24], [25]. FPGA processing times are on the order of nanoseconds, while the other platforms have times in the order of milliseconds. It can also be concluded that the use of the GPU is only advantageous when the number of sequential filters is high, under these circumstances, the FPGA is advantageous. Unlike conventional processors or microcontrollers, FPGAs do not have predefined functions. Instead, they contain many small logic elements, the interconnections and operating principles of which are defined by the user as needed, using programming languages such as VHDL or Verilog.

The purpose of this research is to critically analyze data processing algorithms and their integration with HPC in 3D and line scanning camera systems for real-time wood processing, focusing on efficiency and accuracy improvements in defect detection, quality control, and automation. This paper aims to fill the identified knowledge gap by comparing FPGA-based systems, emphasizing existing applications parameters. This research is developing an advanced 3D and line-scanning camera system concept for real-time wood defect detection and labelling. compare the detection of defects that appear on board or logs (cracks, knots, sapwood, ambrosia wood, and wood rays). It is important to emphasize that all the differences are more or less slight, but the industrial scanner very poorly detects ingrown bark and wood ray. To maximize wood processing, accurate wood defect detection is essential. High-performance computing (HPC) technologies and FPGA-based (Field-Programmable Gate Array) approach for real-time processing solution could serve a critical role, starting from the initial phases of the sawmill processing of logs into sawn boards (or sequential board cross-cutting post process), to the control check for building wood beams, to the classification of wood flooring boards into different classes, etc. The three critical factors were identified for concept: the laser triangulation method which is suitable for determining the direction of wood fibers and resin content, as it provides high accuracy and is able to detect changes in fiber direction based on the dispersion of the laser point. Line scanning technology with controlled LED illumination that ensures stable acquisition of visual information, which allows accurate defect identification of wood surfaces. And the use of FPGA chips for real-time data processing that significantly increases the scanning speed, allowing the integration of both 3D and visual data processing in one system.

II. SPECIFICATIONS OF ENVIRONMENT

Determining the direction of wood fibers based on laser beam scattering is possible only for coniferous species. Deciduous trees have a significantly denser cell structure, so the laser method is not effective in deciduous trees. The bonding of individual wood segments is important because, for example, in systems designed for splitting wood for joining, it is necessary to avoid bonded segments in places where the wood needs to be glued as a result of elongation. Bonded areas do not lend themselves to bonding - due to the reduced strength of the glue and the joint. At the same time, it is possible that the FPGA processor is able to control the direction of the fibers with sufficient resolution.

By performing a detailed analysis of optical and electronic components, the optimal laser and illumination configurations were determined:

- The laser wavelength of 650–750 nm provides the best contrast on different types of wood.
- The dispersion of the laser point in the direction of the wood fiber depends on the density and surface structure of the material, and its mathematical modeling confirmed the possibility of using this parameter to determine the fiber direction.
- The possible use of the laser is also to determine the roughness of the surface with a narrow-angled laser beam. At the same time, the determination of roughness with a laser beam is limited only to materials that are calibrated (planed) and have flat, orthogonal surfaces. The method is not applicable to surfaces that are profiled - moldings, etc.
- The spectral correction of the line-scanning LED illumination reduces unwanted reflections and ensures more accurate defect recognition.

III. FPGA (FIELD-PROGRAMMABLE GATE ARRAY) TECHNOLOGY COMPARISON

For wood processing companies, the ability to detect defects in products and quality is not the only parameter for application but also affordability of the most optimal solution for obtaining maximum value from each product, as well as ensure autonomous operation of the product line. FPGA (Field-Programmable Gate Array) technology research, with practical analysis of costs and opportunities – Table 1 and 2.

TABLE 1 FPGA TECHNOLOGY COMPARISON

System	Developments complexity and prototyping	FPGA and performance	Trigger and synchronization opportunities	Built-in CPU	Availability and costs	Errors test and simulation
OptoMotive Smilodon 10G EVO	*Medium– difficult :* High class FPGA development with UltraScale + FPGAs; opened architecture , difficult for full for adaptation	*Zynq UltraScale + (Kria K26):* >50% FPGA free ; 5–25MP@ high FPS; suitable for powerful processing algorithms and CNNs	*Excellent :* Progressive trigger I/O; two 10GbE interfaces multi-camera synchronization ; precise microseconds level management .	*Yes :* Quad-core ARM Cortex-A53 and dual-core real-time R5; supports imbedded data processing .	*Commercial available :* New product , available after request; high costs , decent delivery time	*Very good :* Supports Vitis/ Vivado environment; AI model simulation ; 10GigE data recording / playback for FPGA design testing .
NI IC-3173	*Very light (NI environment):* Using LabVIEW or Vision Builder AI; medium difficult for coding with C++ or HDL.	*Kintex-7 160T:* Allows sophisticated image processing ; possible AI on FPGA or CPU; precise FPGA control .	*Excellent :* 4 x PoE GigE and isolated digital I/O lines ; precise hardware triggers ; EtherCAT /PLC synchronization .	*Yes:* 2.2 GHz Intel i7 dual-core CPU + 8 GB RAM; working with Windows or NI Linux RT; full PC functionality for analysis .	*Limited :* Not produced (replaced with newer models); available at distributors; initially high price	*Very good :* FPGA simulation and error in LabVIEW environment; Opportunity to test system on PC before applicaiton
Gidel HawkEye 20GigE	*Medium:* Single API image acquisition; FPGA programming with Gidel tools requires experience , but many IP modules available	*Arria 10 (160K/480K):* 20 Gb/s throughput (two 10Gb cameras); large FPGAs resources for parallel processing , also for small AI models .	*Outstanding :* 2x SFP+ inputs cameras; wide GPIO connection point trigger for management ; ideal for precise synchronization .	*None (uses PC CPU):* Works like PCIe FPGA accelerator map; host PC required high level processing .	*Commercial available :* Available straight from Gidel; very high costs ; specialized , but quickly available product .	*Very good :* Errors tested with Gidel ProcVision tools ; image data recording and playback in PC environment; FPGA output validation against CPU program results .

Source: (Zippy Vision SIA data).

Considering that the paper is going to work with FPGA programming, cameras with a closed module (closed FPGA module) have been excluded from the selection, giving preference to cameras that are with an open one. Thus, the focus is currently on starting programming using Vivado tools, which are available for free and focusing on the capabilities of the OptoMotive T-Rex EVO camera.

It should be noted that an important position is debugging capabilities on a computer before transferring algorithms to the FPGA processor, so the next step chosen is Vivado with algorithm testing on a PC.

When evaluating cameras, the triggering and synchronization capabilities are also important. The system basically works with two-channel encoder inputs and it is important that the FPGA chip is able to provide synchronization to other cameras, for example, using only an increasing position trigger.

TABLE 2 FPGA TECHNOLOGY COMPARISON

System	Developments complexity and prototyping	FPGA and performance	Trigger and synchronization opportunities	Built-in CPU	Availability and costs	Errors test and simulation
Techway DragonEYE	*Medium – easy :* Available C++ API, HLS support ; ready to open modules for immideate to start .	*Artix-7/Zynq FPGA:* Real-time several camera (4CH GigE) processing ; possible small AI model Zynq version .	*Very good :* 4xGigE , GPIO trigger signals ; precise synchronization .	*Additionally :* “Smart” version ARM dual-core CPU (Zynq); Lite version no CPU.	*Commercial available :* Available at distributed (1–2 week delivery); medium costs .	*Good:* HLS C simulation ; testing on PC or ARM (Zynq), Vivado error tools
Photonfocus photon3D	*Very easy:* FPGA programming notnecessary ; used as usual GigE camera .	*Specialized FPGA (closed):* Laser lines determination up to 10k	*Excellent :* Built-in encoder interface , <µs trigger precision ; specially designed laser for triangulation .	*None (uses PC):* Works like a camera ; additional analysis is forwarded to computer .	*Commercial available :* Standard product ; delivery from warehouses or branches week	*Not relevant :* Included algorithms are pretested and fixed ; error are done on PC through

		profiles /s; AI not available on camera level			time ; high costs .	GenICam interface and GUI.
OptoMotive T-Rex EVO	*Medium:* Necessary Vivado FPGA development , but is ready-made IP design template ; typical usage, quick realization .	*Zynq-7020 SoC:* ~50% FPGA logic free ; 2MP @ 331 FPS; possible realize simple CNN models .	*Excellent :* 21 ns trigger time distinctive different taking modes; programmable I/O lines for synchronization .	*Yes:* ARM dual core CPU (Linux) embedded in cameras; possible to install user programs on cameras .	*Commercial available :* Available at partners (Pyramid ,Sundance); rather affordable price for beginners level camera	*Very good :* Algorithm testing on ARM level ; FPGA simulation in Vivado environment; CPU and FPGA logic mutual validation .

Source: (Zippy Vision SIA data).

Laser triangulation systems benefit from FPGA-based processing for real-time extraction of laser line or point data. Below are several industrial-grade FPGA solutions (from multiple suppliers) that support GigE industrial cameras, along with their key specifications and suitability for laser triangulation (and laser point distribution). Each is designed for high-speed, real-time operation in rugged environments, and pricing is noted where available

IV. Solution

This makes it suitable for large-scale laser triangulation systems (such as scanning large objects with multiple lasers/cameras in parallel).

Industrial Considerations: Gidel's frame grabbers are typically used inside industrial PCs or edge servers. They adhere to standard PCIe form factors and support Windows and Linux OS environments They provide GPIO (trigger IO, encoders, etc., with opto-isolated and high-voltage tolerance options) on a dedicated connector for integration with external equipment . While the cards themselves rely on the host's environment (cooling, enclosure), they are built for 24/7 operation and high reliability in demanding applications like semiconductor inspection, defense imaging, and 3D vision.

Pricing & Availability: Gidel products are available directly through Gidel. These are highly specialized pieces of hardware; pricing is typically **on request** and varies with the FPGA model and memory configuration. Expect the cost to be significant – on the order of several thousands of dollars or more for toptier models – reflecting the cutting-edge bandwidth and FPGA capability. Gidel does, however, emphasize that using their solution can lower overall system cost in multi-camera setups by removing CPU bottlenecks and reducing the number of PCs needed. For developers needing maximum performance and willing to program FPGAs at a low level, Gidel's solutions provide an **ultra-high-speed platform** well suited for real-time laser triangulation across many cameras or very high resolution (table 3 for summary).

TABLE 3 FPGA TECHNOLOGY SUMMARY COMPARISON

Parameter	Techway DragonEYE	Photonfocus photon3D	OptoMotive T-Rex EVO	OptoMotive Smilodon 10G EVO	NI Industrial Controller	Gidel HawkEye 20GigE
FPGA Model	Xilinx Artix-7	Integrated FPGA (specific model not specified)	Xilinx Zynq-7020 SoC	Xilinx Zynq UltraScale+ MPSoC	Xilinx Kintex-7	Intel Arria 10
Onboard CPU	None (relies on host PC's CPU)	None (dedicated FPGA for image processing)	Dual-core ARM Cortex-A9 processor integrated within Zynq-7020 SoC	Quad-core ARM Cortex-A53 processor integrated within Zynq UltraScale+ MPSoC	Intel Core i7 processor	None (relies on host PC's CPU)
CPU Capabilities	N/A	N/A	Runs Linux OS; handles higher-level tasks, communication,and control functions	Runs Linux OS; manages complex tasks, communication, and advanced processing	Runs NI Linux RealTime OS; Suitable for Complex real-time applications and communication	N/A
Camera Interface	GigE Vision (4 ports)	GigE Vision or 10GigE	GigE Vision	10GigE Vision or GigE Vision	4xGigE Vision	2x10GigE Vision
Resolution	Dependent on connected cameras	1280 to 2048 pixels width	Up to 2048x2048 pixels	Up to 5120x5120 pixels (25 MP)	Dependent on connected cameras	Dependent on connected cameras

Integrated Processing	Yes (user programmable via Vivado HLS)	Yes (built-in laser line detection algorithms)	es (FPGA peak detection core for laser triangulation)	Yes (high-performance FPGA for real-time processing)	Yes (programmable via LabVIEW FPGA)	Yes (user programmable FPGA for real-time processing)
I/O and Synchronization	Yes (trigger inputs, GPIO)	Yes (isolated inputs/outputs)	Yes (isolated inputs/outputs)	Yes (isolated inputs/outputs)	Yes (isolated inputs/outputs)	Yes (GPIO, isolated inputs/outputs)
Industrial Environment	Yes (PCIe card suitable for industrial applications)	Yes (robust housing designed for industrial use)	Yes (compact and robust housing for industrial environments)	Yes (robust housing suitable for industrial environments)	Yes (IP67-rated, fanless design for harsh industrial conditions)	es (PCIe card designed for 24/7 operation in industrial settings)
FPGA Programming Language	VHDL, Verilog, and High-Level Synthesis (HLS) tools like Vivado HLS	Not specified (likely Proprietary firmware; user programmability may be limited)	VHDL, Verilog, and HLS tools like Vivado HLS	VHDL, Verilog, and HLS tools like Vivado HLS	LabVIEW FPGA (graphical programming environment)	VHDL, Verilog, and High-Level Synthesis tools
FPGA Processor Capabilities	Artix-7 FPGA with sufficient resources for realtime image processing	Integrated FPGA optimized for laser line detection; specific capabilities not detailed	Zynq-7020 SoC combining dual-core ARM Cortex-A9 processor with FPGA fabric for real-time processing	Zynq UltraScale+ MPSoC with quad-core ARM Cortex-A53 processor and large FPGA fabric for highperformance tasks	Kintex-7 FPGA with ample resources for complex real-time processing tasks	Arria 10 FPGA offering high logic density and DSP blocks for intensive real-time processing
Approximate Price	Available upon request	Approximately \$3,000–\$7,000 USD	Approximately \$3,000–\$6,000 USD	Approximately \$6,000+ USD	Approximately \$10,000+ USD	Available upon request (typically several thousand USD)

Source: (Zippy Vision SIA data).

The used application combines multiple simultaneous tasks using a single FPGA camera (**OptoMotive T-Rex EVO as chosen from Table 3**):

1. **3D Laser Triangulation** (laser dots to measure depth)
2. **Laser Dot Distribution Analysis** (for fiber-direction mapping)
3. **Color Line Scanning** (triggered precisely via encoder signals)

Camera's sensor will be logically divided into separate areas (regions of interest – ROIs), each used for a different purpose:

• **Sector 1:** Laser dots (3D triangulation & distribution analysis)

• **Sector 2:** Color line scanning (high-resolution colour capture)

All data will be pre-processed onboard the FPGA and ARM CPU (Linux OS), enabling fast real-time decisions and reduced data transfer Figure 1.

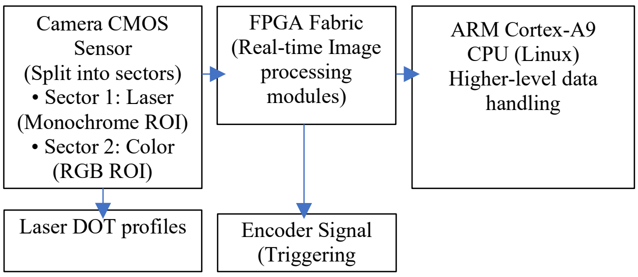

Fig. 1. Conceptual Hardware-Software Diagram

The FPGA can be used to perform inline processing on images acquired from these cameras (for example, filtering, thresholding, or even laser line extraction algorithms) before passing results to the host CPU or control logic. This co-processing offloads the CPU and can greatly reduce latency in a triangulation system.

Explanation of FPGA-based Processing Workflow

1. Sensor Acquisition

The camera sensor captures images simultaneously:

- Monochrome sector (laser dot patterns)
- Color sector (RGB image line scan)

2. FPGA-Based Real-time Pre-processing

Custom FPGA modules process the data in parallel:

- Laser Triangulation Module: identifies laser dot positions and calculates heights for 3D reconstruction.
- Dot Distribution Module: analyses laser dot distribution, generating a fiber direction map.
- Color Line Module: acquires RGB colour line data, synchronised by encoder signal.

3. ARM CPU Higher-Level Processing (Linux)

Processed data from FPGA passed to the onboard ARM Cortex-A9 CPU for:

- Data aggregation and timestamping.
- Higher-level algorithms (e.g., detailed fibre direction analysis, quality checks).
- Networking (sending processed data to host PC).
- Integration and communication with external devices/systems (e.g., ERP systems).

4. Data Transfer to Host PC

Reduced datasets (height profile, fibre maps, colour scans) are sent via GigE to a PC for:

- Long-term storage.

- Visualization.
- Advanced analytics and reporting.
- Integration with MES/ERP systems.

V. TESTING RESULTS

During testing period image acquisition stability tested under different lighting conditions – 100 lux was performed,
500 lux, 1000 lux, 3000 lux. The actual level at which the sensor works and is able to unambiguously recognize the laser shape is up to 1000 lux. At higher lighting levels, sensor data and laser line extraction are difficult:
• data flow quality and noise level in the sensor tested;
• triggering accuracy validated for synchronization with external line scanning systems;
• operation of FPGA processing-based algorithms tested on real sensor data.

For the initial development, testing and creation of new algorithms, the Intel Questa FPGA simulation environment was used, which can execute HDL code and is compatible with the Vivado architecture. After further research, it was decided to use the Zynq Ultrascale+ MPSoC Development Board for further development, which allows for the creation of an integrated camera system, which is further compatible with the integrated camera candidates identified in the first stage. The reason for this choice is the wider programming capabilities of FPGA, where the final software tests will allow for the use of various types of industrial cameras. A technical evaluation report of camera models has been created, which summarizes the most important parameters that served as the basis for hardware selection (based on the previously developed comparative table from the application material). Additional research has found that it is more cost-effective to carry out the initial development with the Zynq Ultrascale+ MPSoC Development Board, which is compatible with the studied cameras at the program and logic level. Hardware compatibility with the planned FPGA programming environment (Xilinx Vivado) and ARM CPU algorithm simulation has been validated, ensuring optimal development speed.

The initial FPGA firmware version has been developed and implemented, which provides data acquisition from the sensor and initial processing in real time (Figure 2).
• The processing throughput level of ~800–200 profiles per second at a resolution of 1000 points has been achieved.
• Full data synchronization between the sensor acquisition clock, encoder pulse signals and external trigger system has been implemented.
• The functionality of the processing blocks has been validated with real sensor data in laboratory conditions.
• A flexible debugging and simulation environment has been provided, which significantly accelerates the development of further algorithms and their transfer to the FPGA. The debugging environment is based on the FPGA processor simulation environment, which simulates the operation of the FPGA processor and allows tracing operation steps and states on test data using the debugging process in the simulation environment. Such debugging is not practical during the operation of an already programmed processor.

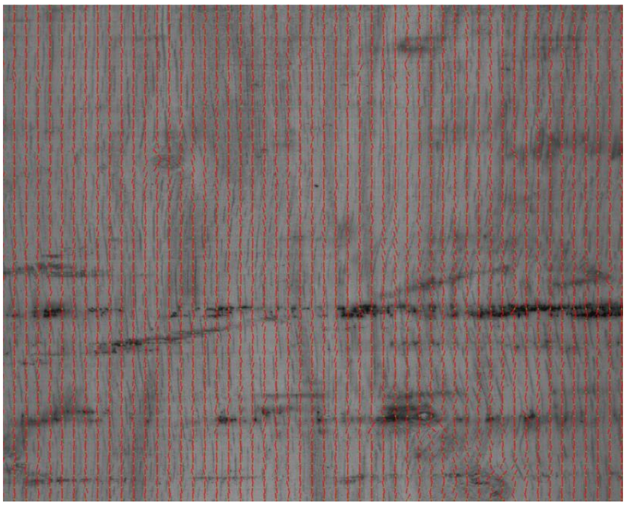

Fig. 2. MExample of fiber directional coverage map (Zippy Vision SIA property).

As part of the project, the phase of identification and evaluation of artificial intelligence (AI) models was initiated with the aim of determining the most optimal segmentation model solutions for wood defect recognition, adapting them to future data sets that will be obtained with the developed 3D and line-scanning camera system.
Taking into account the visual and structural characteristics of wood defects (high defect diversity, uneven shapes, the impact of different fiber orientations on the visual image), a detailed analysis of the literature and current technological sources on the development of segmentation algorithms was carried out:

- Transformer architectures were evaluated: Vision Transformer (ViT), Swin Transformer, Mask2Former, Segment Anything Model (SAM).
- The advantages of these models in segmentation tasks with wood materials were compared:
- The ability to specialize these models with a limited number of samples, with the aim of: segment complex surface textures; distinguish changes in fiber direction and surface damage volumes; process high-resolution images.

To detect gumminess and small cracks, create a differential algorithm that uses laser width and intensity data and creates a differential data matrix that allows for reproducing gumminess and crack identification. Considering that physical variations are known for both gumminess and cracks, an augmentation algorithm has been developed that allows for generating artificial surface textures (Figure 3).

Artificial surface textures are necessary because finding mathematical parameters for crack and gumminess recognition is considered less robust and more time-consuming than creating augmented data and searching for parameters through the AI training process. Augmented data does not require any interpolation, as the segment area is known at the time of augmentation.

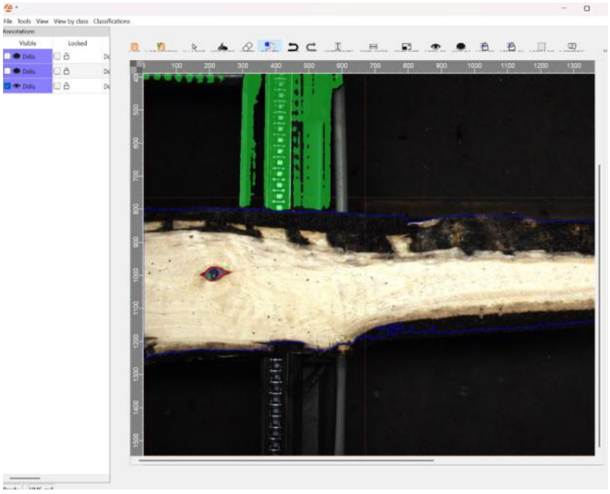

Fig. 3. The result of automatic segmentation on the board image, using the semantic segmentation SAM model on a real-life image (Zippy Vision SIA property).

The Segment Anything Model was chosen due to its simpler integration into a new flow.

The following was found during the research:

- Large transformer models have significantly higher hardware requirements and lower speeds than those allowed in high-speed and high-performance scanners.
- Large models have significantly higher initial accuracy on a limited amount of annotation data, such as the U-Net model, which can be used on end-user hardware with a smaller number of annotations.
- The integration of large models into the annotation and model development flow significantly accelerates AI accuracy and reduces costs, as large models are excellent for creating initial annotations, and a new AI processing flow has been launched in which large models are integrated as a distillation source.

VI. CONCLUSIONS

For FPGA programming, the possibility of initial simulation is essential, taking into account that after the algorithms themselves are transferred to the FPGA processor program, the possibilities for further development, testing and debugging are limited. The chosen solution optimally combines the necessary hardware programmability, processing power and flexibility in real-time data flow management. Such a base allows in the next stages to implement both experimental 3D profile processing, AI model data preparation, and further optimization of laser triangulation and line scanning systems. This activity result directly corresponds to the goal of the project application to create an effective camera platform base capable of realizing combined visual and 3D information acquisition for a wood defect recognition system. The developed initial FPGA firmware version fully confirms the compliance of the selected platform with the technical requirements of the scalability. The implementation of 3D profile generation and calibration algorithms, laser point scattering analysis for fiber direction determination and real-time calculation blocks for the initial geometry of defects are allowing to build a system with necessary high-speed precision. These results bring the wood processing sector significantly closer to achieving its goal — to provide high-precision combined 3D and visual information processing in real time, which is applicable for automatic recognition and marking of wood defects in industrial production. The calibration stage of the implementation of laser triangulation and line scanning integration is creating a functioning experimental system that combines both information acquisition technologies into a single synchronized flow. The synchronous 3D and visual data obtained in this way create a basis for the development of high-precision wood defect recognition algorithms and further training of AI models.

The achieved results directly correspond to the defined main goal of the paper to develop a new generation of combined camera system that integrates elements of laser triangulation, line scanning and artificial intelligence in wood quality control automation. The conducted segmentation-based model research has provided a solid foundation for adapting artificial intelligence algorithms to the specific problem of wood defect identification. The choice of Transformer architecture provides significant advantages for companies by delivering higher accuracy in processing irregular defect contours; accelerated development time of specialized models; accelerated and refined implementation of annotations using SAM models at all stages of the workflow. Modern architectures trained using the new workflow model are able to model structural and visual aspects of the wood surface simultaneously with better adaptation capabilities to increase data volume.

The prepared methodology and solution allow for the wood processing sector to start practical applications for model training in the subsequent stages of the development, using the proposed innovative 3D and line-scanning camera combined solution, capable of simultaneously capturing both visual and 3D information, as well as identifying wood properties such as fiber direction and resin accumulation.

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